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09/895,218	07/02/2001	Brian Gaudet	0023-0036	8537

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EXAMINER	
HABTE, ZEWDU	
ART UNIT	**PAPER NUMBER**
2661	

DATE MAILED: 04/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/895,218	GAUDET, BRIAN
	Examiner	Art Unit
	Zewdu Habte	2661

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *8-21* is/are allowed.

6)☒ Claim(s) *1-3, 5-7, 22-24, 26-29* is/are rejected.

7)☒ Claim(s) *4 and 25* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 7, 14 are objected to because of the following informalities:

In claim 7, line 3, the word "stored" should be changed to –store-.

In claim 14 line 3, "the second data path" should be changed to –a second data path–.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

3. Claim 1 recites the limitation "Q packets" in lines 7 and 9. There is insufficient antecedent basis for this limitation in the claim.

4. Claim 2 recites the limitation "Q packets" in line 3. There is insufficient antecedent basis for this limitation in the claim.

5. Claim 5 recites the limitation "Q packets" in line 2. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1, 2, 7, 22, 23, 26, 27 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kanazashi (US 2001/0012290).

As to claim 1, Kanazashi discloses a method of converting a first data path [an input data path to input buffer 10] carrying P... per processing cycle [maximum number of data input buffer 10 accommodates from the input data path at one time (P) equals processing cycle to occupy buffer 10] to a second data path [Fig. 5, data bus A0, A1, A2, A3] carrying N ... per processing cycle [as illustrated in Fig. 5, selector 12 selects N0-N3 (N = 4 data processes at one time or 4 data per processing cycle)], wherein N< P [4< P (since it is stated that 4 is less than P, the buffer size is 2^3...n)], comprising:

receiving the P ... during a first processing cycle [Fig. 5, input buffer 10 (maximum buffer capacity reached that is equal to P at first processing cycle)] on the first data path;

storing the P ... in a queue [Fig. 5, input buffer 10 (queue)];

shifting first data from the queue into a shift register [Fig. 5, shift register 14 (shifts N0-N3 data in the shift register)];

selectively retrieving data from the shift register until a first set of Q ... [Fig. 5, N0-N3 (a first set of N = Q data)] of the P ... is retrieved [pg. 2, par. 31, lines 18+, selector 12 selects N0-N3 data to transmit from the shift register by following the address signal respectively (selectively)]; and

sending the set of Q ... on the second data path during the first processing cycle [Fig. 5, data bus A0, A1, A2, A3 (until the input buffer 10 is empty and starts receiving data, the transmission of these data is in the first processing cycle)].

Although "data" instead of "packets" is used in Kanazashi's teaching, one of ordinary skill in the art would recognize that "packet" is an obvious form of data.

As to claim 2, Kanazashi discloses shifting second data from the queue into the shift register; selectively retrieving data from the shift register until a second set of Q packets of the P packets is retrieved; and sending the second set of Q packets on the second data path during a second processing cycle [(implicitly taught because the data processing system continues cyclically to process the second data set the same as the first data set is processed)].

As to claim 7, Kanazashi discloses a ... processing system [Fig. 5], comprising:

a first data path [Fig. 5, input data path to input buffer 10] configured to receive P ... during a first processing cycle [maximum number of data input buffer 10 accommodates from the input data path at one time (P) equals a first processing cycle to occupy buffer 10];

a queue [Fig. 5, input buffer 10 (queue)] configured to stored the P received ... [Fig. 5, input buffer 10 (maximum buffer capacity is equal to P)];

a shift register [Fig. 5, shift register 14 (shifts N0-N3 data in the shift register)]; and

a control unit [Fig. 5, selector 12, and CLK1] configured to:

shift data of the P ... from the queue into the shift register [pg. 2, par. 31, lines 15-18, (data from the buffer is moved to shift register 14 using an internal CLK1 and input selector 12 to select data input to the shift register)]

selectively retrieve data from the shift register until a first set of Q ... [Fig. 5, N0-N3 (a first set of Q data)] is retrieved [pg. 2, par. 31, lines 18+, selector 12 selects N0-N3 data to transmit from the shift register by following the address signal respectively (selectively)] , wherein Q < P [(Q = 4, and 4< P (since it is stated that 4 is less than P, the buffer size is 2^3...n)], and

send the first set of Q ... on a second data path [Fig. 5, data bus A0, A1, A2, A3] during the first processing cycle [Fig. 5, data bus A0, A1, A2, A3 (until the input buffer 10 is empty and starts receiving new data, the transmission of these data is in the first processing cycle)].

Although "data" instead of "packets" is used in Kanazashi's teaching, one of ordinary skill in the art would recognize that "packet" is an obvious form of data.

As to claim 22, Kanazashi discloses a method of processing a plurality of ... [maximum number of data input buffer 10 accommodates] using a single ... per cycle processing device [Fig. 5, a set of data N0-N3], comprising:

receiving the plurality of ... during a first processing cycle[Fig. 5, input buffer 10 (maximum buffer capacity reached at first processing cycle)];

storing the plurality ... in a queue [Fig. 5, input buffer 10 (queue)];

shifting a first quantity [Fig. 5, N0-N3] of data from the queue into a shift register [Fig. 5, shift register 14 (shifts N0-N3 data in the shift register)];

selectively retrieving data from the shift register until a first set of ... [Fig. 5, N0-N3 (a first set of N = Q data)] of the plurality of ... is retrieved [pg. 2, par. 31, lines 18+,

selector 12 selects N0-N3 data to transmit from the shift register by following the address signal respectively (selectively)]; and

processing retrieved first ... during the first processing cycle [Fig. 5, data bus A0, A1, A2, A3 (until the input buffer 10 is empty and starts receiving data, the transmission of these data is in the first processing cycle)].

Although "data" instead of "packets" is used in Kanazashi's teaching, one of ordinary skill in the art would recognize that "packet" is an obvious form of data.

As to claim 23, Kanazashi discloses selectively retrieving data from the shift register until a second packet of the plurality of packets is retrieved; and processing the retrieved packets on the second data path during a second processing cycle [(implicitly taught because the data processing system continues cyclically to process the second data set the same as the first data set is processed)].

As to claim 26, Kanazashi discloses a processing device [Fig. 5] that is configured to process only one packet per processing cycle processes the first packet during the first processing cycle [Fig. 5, a set of data N0-N3].

As to claim 27, Kanazashi discloses processing device that is configured to process only one packet per processing cycle processes the second packet during the second processing cycle [(implicitly taught because the data processing system continues cyclically to process the second data set the same as the first data set is processed)].

As to claim 29, Kanazashi discloses a ... processing system [Fig. 5], comprising:

a first data path [Fig. 5, input data path to input buffer 10] configured to receive a plurality of ... during a first processing cycle [maximum number of data input buffer 10 accommodates equals a first processing cycle to occupy buffer 10];

a queue [Fig. 5, input buffer 10 (queue)] configured to stored the plurality of ... [Fig. 5, input buffer 10 (maximum buffer capacity)];

a control unit [Fig. 5, selector 12, and CLK1] configured to:

shift a first quantity [Fig. 5, N0-N3] of data of the plurality of ... from the queue into the shift register [pg. 2, par. 31, lines 15-18, (data from the buffer is moved to shift register 14 using an internal CLK1 and input selector 12 to select data input to the shift register)]

selectively retrieve data from the shift register until a first ... [Fig. 5, N0-N3 (a first data)] is retrieved [pg. 2, par. 31, lines 18+, selector 12 selects N0-N3 data to transmit from the shift register by following the address signal respectively (selectively)], and

a ... processing device [Fig. 5] configured to process the retrieved first ...during the first processing cycle [Fig. 5, data bus A0, A1, A2, A3 (until the input buffer 10 is empty and starts receiving new data, the transmission of these data is in the first processing cycle)].

Although "data" instead of "packets" is used in Kanazashi's teaching, one of ordinary skill in the art would recognize that "packet" is an obvious form of data.

8. Claims 3 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kanazashi as applied to claims 1 and 22 above, and further in view of Ackland et al. (US 5220325).

As to claim 3, Kanazashi does not teach the queue is a first-in-first-out queue, but Ackland discloses an input FIFO 405 as illustrated in Fig. 4. It would have been obvious to one of ordinary skill in the art to combine Kanazashi with Ackland for the purpose of having an input FIFO buffer in a data processing system. The motivation is to provide data to the shift register at a uniform rate, which is determine by the clock.

As to claim 24, Kanazashi does not teach the queue is a first-in-first-out queue, but Ackland discloses an input FIFO 405 as illustrated in Fig. 4. It would have been obvious to one of ordinary skill in the art to combine Kanazashi with Ackland for the purpose of having an input FIFO buffer in a data processing system. The motivation is to provide data to the shift register at a uniform rate, which is determine by the clock.

9. Claims 6 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kanazashi as applied to claims 1 and 22 above, and further in view of Howson (US 33900, Reissue of 4397020).

As to claim 6, Kanazashi does not disclose a cyclical redundancy checker, CRC, but Howson discloses a device to monitor CRC (abs. lines 1-2). It would have been obvious to one of ordinary skill in the art to combine Kanazashi with Howson for the purpose of having a CRC device in order to monitor input data. The motivation is to detect if there is any delay in the data stream to contradict with the original data.

As to claim 28, Kanazashi does not disclose a cyclical redundancy checker, CRC, but Howson discloses a device to monitor CRC (abs. lines 1-2). It would have been obvious to one of ordinary skill in the art to combine Kanazashi with Howson for the purpose of having a CRC device in order to monitor input data. The motivation is to detect if there is any delay in the data stream to contradict with the original data.

Allowable Subject Matter

10. Claims 4, 25 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

11. Claims 8-21 allowed.

As to claim 8, ...determining whether the data in the shift register comprises at least one of an end-of-packet indicator, a data field, and a start-of-packet indicator; and sending, based on the determination, a first set of Q packets on a second data path during the first processing cycle.

As to claim 13, ...determine whether the data in the shift register comprises at least one of an end-of-packet indicator, a data field, and a start-of-packet indicator, and send, based on the determination...

As to claim 14, ...converting the plurality of packets on the first data path to a second packet on the second data path...

As to claim 21, ...convert the received P packets on the first data path to a second set of Q packets on the second data path during a second processing cycle; and a first processing device....

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zewdu Habte whose telephone number is 571-272-3115. The examiner can normally be reached on 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chau T Nguyen can be reached on 571-272-3126. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Zewdu Habte (Zed)
Examiner
Art Unit 2661

ZH
April 4, 2005

KENNETH VANDERPUYE
PRIMARY EXAMINER